CLAIMS

What is claimed is:

1. A method, comprising:

receiving a pair of input clock signals;

utilizing a stratum clock state machine to control a multiplexer;

utilizing the multiplexer to switch an input of a main clock between each of the pair of input clock signals;

inducing a phase build-out activity; and

transmitting an output clock signal.

2. The method of claim 1, wherein inducing the phase build-out activity includes eliminating a set of input transients.

3. The method of claim 1, further comprising utilizing the stratum clock state machine to manage a plurality of phase-locked loops.

4. The method of claim 1, further comprising utilizing the stratum clock state machine to set the main clock to a main clock normal state

5. The method of claim 1, further comprising utilizing the stratum clock state machine to set the main clock to a main clock freerun state.

6. The method of claim 1, further comprising utilizing the stratum clock state machine to set the main clock to a main clock holdover state.

7. The method of claim 6, further comprising activating the phase buildout activity.

8. The method of claim 6, further comprising applying a frequency history to a frequency synthesizer in the main clock.

9. The method of claim 8, wherein applying the frequency history includes applying an approximately twenty-five second frequency history.

10. The method of claim 8, further comprising forcing a phase measurement circuit into a zero phase error state by preloading a phase measurement counter with a zero substantially on an edge of an input signal.

11. The method of claim 1, further comprising utilizing the stratum clock state machine to select a short time constant filter in the main clock.

12. The method of claim 1, further comprising utilizing the stratum clock state machine to select a long time constant filter in the main clock.

13. The method of claim 1, further comprising utilizing the stratum clock state machine to select a programmable filter.

14. The method of claim 1, further comprising providing the stratum clock state machine with a user selection input, wherein the user selection input includes at least one member selected from the group consisting of: a select freerun mode, a select reference A mode, a select reference B mode and a select holdover mode.

15. The method of claim 1, further comprising setting the stratum clock state machine in a state including at least one member selected from the group consisting of: a stratum clock state machine normal state, a stratum clock state machine freerun state, a stratum clock state machine switch state, a stratum clock state machine offset state and a stratum clock state machine holdover state.

16. The method of claim 1, further comprising providing the stratum clock state machine with a frequency offset input including:

receiving a frequency offset signal produced by each of a pair of input digital phase-

locked loops; and

measuring the frequency offset signal.

17. The method of claim 16, further comprising setting the stratum clock state machine to the stratum clock state machine offset state if a measured frequency offset signal is greater than approximately 2.4 parts per million.

18. The method of claim 17, further comprising maintaining the stratum clock state machine offset state for approximately an additional 12 seconds after the measured frequency offset signal is de-asserted.

19. The method of claim 1, further comprising providing the stratum clock state machine with a frequency error input including:

receiving a frequency error signal produced by each of the pair of input digital phase-locked loops; and

measuring the frequency error signal.

20. The method of claim 19, further comprising setting the stratum clock state machine to a stratum clock state machine holdover state if a measured frequency error signal is greater than approximately 14.4 parts per million.

21. The method of claim 20, further comprising applying an approximately twenty-five second frequency history to the frequency synthesizer in the main clock.

22. The method of claim 1, further comprising providing the stratum clock state machine with a phase step input including:

receiving a phase step signal produced by each of the pair of input digital phase-locked loops; and

measuring the phase step signal.

23. The method of claim 22, further comprising setting the stratum clock state machine to the stratum clock state machine holdover state if a measured phase step signal is greater than approximately 1.4 microseconds.

24. The method of claim 23, further comprising performing a phase buildout function for approximately 12 seconds.

25. The method of claim 1, further comprising providing a set of three timers, wherein each timer is set by a state machine input event, including: a phase buildout timer, a hold timer, and a skip timer.

26. The method of claim 25, further comprising clearing the set of three timers when a reference switch is detected.

27. A computer program, comprising computer or machine readable program elements translatable for implementing the method of claim 1.

28. An apparatus for performing the method of claim 1.

29. A field programmable gate array for performing the method of claim 1.

30. An application specific integrated circuit for performing the method of claim 1.

31. An apparatus, comprising:

a first input clock digital phase-locked loop;

a second input clock digital phase-locked loop;

a stratum clock state machine coupled to the first input clock digital phase-locked loop and to the second input clock digital phase-locked loop; and

a main clock phase-locked loop coupled to the first input clock digital phase-locked loop, to the second input clock digital phase-locked and to the stratum clock

state machine.

32. The apparatus of claim 31, wherein the stratum clock state machine can define a holdover state in which a phase buildout function is active.

33. The apparatus of claim 32, wherein the stratum clock state machine can define a normal state, an offset state, a switch state and a freerun state.

34. The apparatus of claim 31, further comprising a numerically controlled oscillator coupled to the main clock phase-locked loop.

35. The apparatus of claim 34, further comprising a phase and frequency detector coupled to the numerically controlled oscillator.

36. The apparatus of claim 35, further comprising an oven controlled crystal oscillator, coupled to the phase and frequency detector.

37. The apparatus of claim 36, further comprising a temperature sensor coupled to the oven controlled crystal oscillator and to the stratum clock state machine.

38. The apparatus of claim 35, further comprising a loop filter coupled to the phase and frequency detector.

39. The apparatus of claim 38, wherein the loop filter includes a programmable filter.

40. The apparatus of claim 39, wherein the programmable filter is coupled to the stratum clock state machine.

41. The apparatus of claim 38 further comprising a voltage controlled oscillator coupled to the loop filter, to the first input clock digital phase-locked loop and to the second input clock

digital phase-locked loop.

42. The apparatus of claim 41, further comprising:
an output buffer coupled to the voltage controlled oscillator; and
a clock divider coupled to the voltage controlled oscillator and to the output buffer.

43. The apparatus of claim 31, further comprising an eight bit parallel bus coupled to the stratum clock state machine.

44. The apparatus of claim 31, further comprising a simple logic interface coupled to the stratum clock state machine.

45. A method comprising deploying the apparatus of claim 31.

46. A kit, comprising the apparatus of claim 31.

47. The kit of claim 46, further comprising instructions.

48. A method comprising deploying the kit of claim 46.